**Constant and high speed adder design using QSD number system**

**ABSTRACT**

 With the binary number system, the computation speed is limited by formation and propagation of carry especially as the number of bits increases. Using a quaternary Signed Digit number system one may perform carry free addition, borrow free subtraction and multiplication. However the QSD number

system requires a different set of prime modulo based logic elements for each arithmetic operation. A carry free arithmetic operation can be achieved using a higher radix number system such as Quaternary Signed Digit (QSD). In QSD, each digit can be represented by a number from -3 to 3. Carry free addition and other operations on a large number of digits such as 64, 128, or more can be implemented with constant delay and less complexity. Design is simulated & synthesized using Modelsim6.0, Microwind and Leonardo Spectrum.

**LANGUAGE USED:**

* Verilog HDL

**TOOLS REQUIRED:**

* MODELSIM – Simulation
* XILINX-ISE – Synthesis